Highly Programmable Linear Hall-Effect Sensor IC

FEATURES AND BENEFITS

- On-board diagnostics
  - □ Broken ground detection
  - □ V_{CC} undervoltage detection
  - □ V_{CC} overvoltage detection
- Customer-programmable offset, sensitivity, polarity, and output clamps
- Integrated power supply and output bypass capacitors
- Customer and factory access code for enhanced reliability
  - □ Factory code required for write access to TC trim and other factory registers
  - □ Customer code required for write access to customer registers

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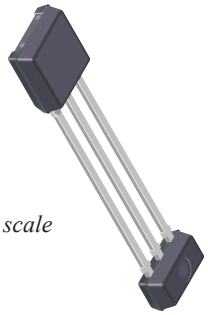
PACKAGE: 3-pin SIP (suffix UC)



Not to scale

DESCRIPTION

The Allegro™ A1377 programmable linear Hall-effect sensor IC is designed for applications that require high accuracy and high resolution without compromising bandwidth. The A1377 employs segmented, linearly interpolated temperature compensation technology. This improvement greatly reduces the total error of the device across the whole temperature range. As a result, the device is ideally suited for sensing in numerous automotive applications, such as linear and rotary position sensors in actuators and valves.

Available in a through-hole, small form factor, single in-line package (SIP), the A1377 Hall-effect sensor IC has a broad range of sensitivity and offset operating bandwidth. The accuracy and flexibility of this device is enhanced with user programmability, via the VCC and output pins, which allows the device to be optimized in the application.

This ratiometric Hall-effect sensor IC provides a voltage output that is proportional to the applied magnetic field. The quiescent voltage output (QVO) is user-adjustable from approximately 5% to 95% of the supply voltage. The device sensitivity is adjustable within the range of 1 to 14 mV/G.

The features of this linear device make it ideal for use in automotive and industrial applications requiring high accuracy, and apply across an extended temperature range, from –40°C to 150°C.

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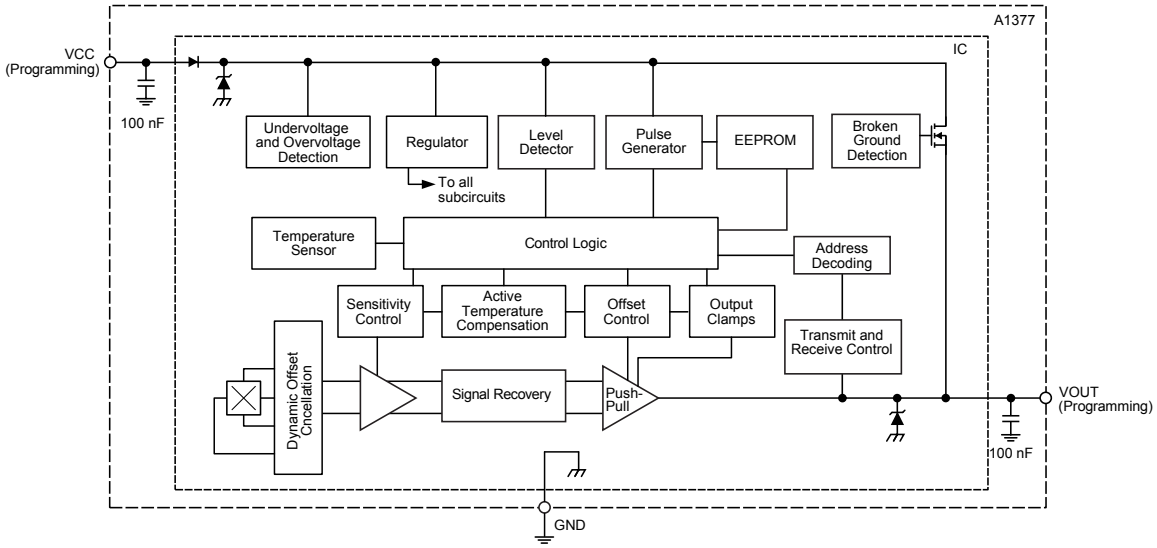


Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Temperature-stable quiescent voltage output and sensitivity: sensitivity temperature coefficient (TC) and QVO temperature coefficient programmed at Allegro for improved accuracy
- Optional output voltage clamps provide short-circuit diagnostic capabilities
- Wide ambient temperature range: –40°C to 150°C
- Enhanced EMC performance for stringent automotive applications

DESCRIPTION (continued)

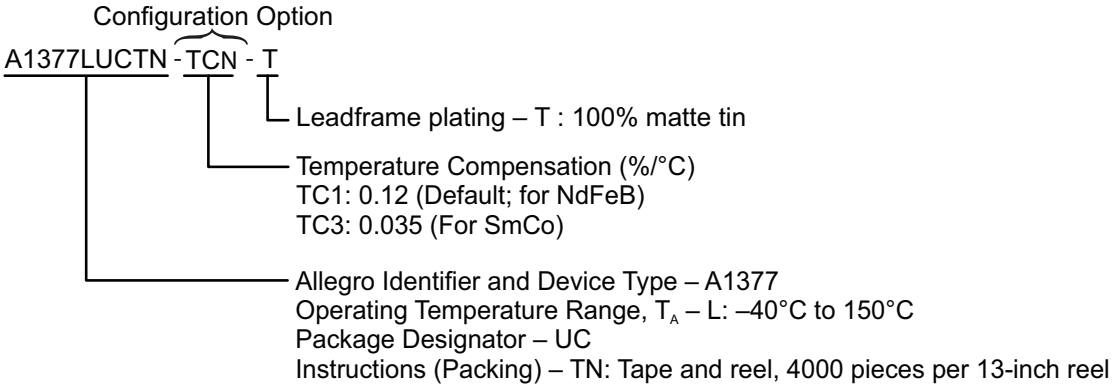
Each BiCMOS monolithic circuit integrates a Hall element, temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, a clamped low-impedance output stage and a proprietary dynamic offset cancellation technique.

The A1377 sensor is provided in a 3-pin single in-line package (UC suffix) with bypass capacitors integrated into the package. It is lead (PB) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Packing*
A1377LUCTN–TC*[N]*–T	4000 pieces per 13-inch reel

*Contact Allegro™ for additional packing options.



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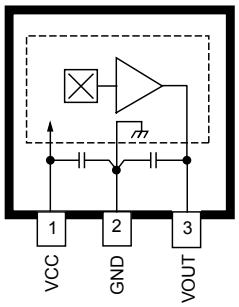
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		16	V
Reverse Supply Voltage	V_{RCC}		–16	V
Forward Output Voltage	V_{OUT}	$V_{OUT} < V_{CC} + 2$	16	V
Reverse Output Voltage	V_{ROUT}	T_J(max) not exceeded	–5	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUT to GND	10	mA
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	–10	mA
Reverse Supply Current	I_{RCC}	At absolute maximum conditions, the device sinks not more than 50 mA	–50	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Estimated, on single-layer PCB with copper limited to solder pads	201	ºC/W

*Additional thermal information available on the Allegro website.



UC Package Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCC	Device power supply, also used for programming
2	GND	Device ground
3	VOUT	Output signal, also used for programming

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OPERATING CHARACTERISTICS: Valid across full T_A range, C_{BYPASS} = 0.1 µF (internal), V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	No load on VOUT	–	7.5	10	mA
Reverse Supply Current	I_{RCC}	V_{CC} = –15 V, T_A = 25°C	–10	–	–	mA
Power-On Time [2]	t_{PO}	T_A = 25°C, $C_{LOAD(PROBE)}$ = 10 pF	–	400	2000	µs
Delay to Clamp [2]	t_{CLP}	T_A = 25°C, C_{LI} = 100 nF	–	30	–	µs
Internal Bandwidth	BW_i	Large signal –3 dB	–	2.5	–	kHz
Chopping Frequency	f_C	T_A = 25°C	–	125	–	kHz
OUTPUT CHARACTERISTICS						
Output Referred Noise [11]	V_N	T_A = 25°C, C_{BYPASS} = open, Sens = 2.5 mV/G, no load on VOUT	–	2.1	6	mV_{RMS}
Input-Referred RMS Noise Density [11]	V_{NRMS}	T_A = 25°C, C_{BYPASS} = open, no load on VOUT, magnetic input signal frequency << BW_i	–	2.5	6	mG/√Hz
DC Output Resistance [11]	R_{OUT}		–	1	100	Ω
Output Load Resistance	R_L	VOUT to VCC	4.7	–	–	kΩ
		VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance (Internal) [3]	C_{LI}	VOUT to GND	–	0.1	–	µF
Output Load Capacitance (External)	C_{LX}	VOUT to GND	–	–	0.47	µF
Propagation Delay [11]	t_{PD}	C_{LX} = 0	–	–	0.5	ms
Response Time [11]	$t_{RESPONSE}$	C_{LX} = 0	–	–	2	ms
Output Saturation Voltage	$V_{OUT(sat)H}$	$R_{PULLDOWN}$ = 4.7 kΩ, CLAMP_HIGH = 0	4.65	4.8	–	V
	$V_{OUT(sat)L}$	R_{PULLUP} = 4.7 kΩ, CLAMP_LOW = 0	–	0.2	0.35	V
PRE-PROGRAMMING TARGET [4]						
Pre-Programming Quiescent Voltage Output	$V_{OUT(Q)init}$	Magnetic Input B = 0 G, T_A = 25°C	–	2.5	–	V
Pre-Programming Sensitivity	$Sens_{init}$	T_A = 25°C	–	6	–	mV/G
Pre-Programming Sensitivity Temperature Compensation [12]	$TC1_{SENSinit}$	T_A = 150°C, calculated relative to T_A = 25°C	–	0.12	–	%/°C
	$TC3_{SENSinit}$	T_A = 150°C, calculated relative to T_A = 25°C	–	0.035	–	%/°C
Pre-Programming Quiescent Voltage Output Drift	$\Delta V_{OUT(Q)}$	T_A = 150°C, calculated relative to T_A = 25°C	–	0	–	mV/°C
Pre-Programming Output Voltage Clamp (High)	$V_{CLP(H)init}$	T_A = 25°C, $R_{PULLDOWN}$ = 4.7 kΩ, CLAMP_HIGH = 0	–	$V_{OUT(sat)H}$	–	V
Pre-Programming Output Voltage Clamp (Low)	$V_{CLP(L)init}$	T_A = 25°C, R_{PULLUP} = 4.7 kΩ, CLAMP_LOW = 0	–	$V_{OUT(sat)L}$	–	V

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
OUTPUT VOLTAGE CLAMP PROGRAMMING						
Output Voltage Clamp (High Range)	$V_{CLP(HIGH)}$	T_A = 25°C, R_L = 4.7 kΩ	2	–	$V_{OUT(sat)H}$	V
Output Voltage Clamp (Low Range)	$V_{CLP(LOW)}$	T_A = 25°C, R_L = 4.7 kΩ	$V_{OUT(sat)L}$	–	3	V
Output Voltage Clamp Programming Bits	$BIT_{CLPHIGH}$		–	9	–	bit
	BIT_{CLPLOW}		–	9	–	bit
Output Voltage Clamp Programming Average Step Size	$STEP_{CLP}$		–	10	–	mV
QUIESCENT VOLTAGE OUTPUT PROGRAMMING						
Typical Quiescent Voltage Output Coarse Adjustment	$V_{OUT(Q)INIT}$	QVO_COARSE = 0, QVO_FINE = 0, Magnetic Input B = 0 G, T_A = 25°C	–	2.5	–	V
		QVO_COARSE = 1, QVO_FINE = 0, Magnetic Input B = 0 G, T_A = 25°C	–	3.5	–	V
		QVO_COARSE = 2, QVO_FINE = 0, Magnetic Input B = 0 G, T_A = 25°C	–	4.5	–	V
		QVO_COARSE = 3, QVO_FINE = 0, Magnetic Input B = 0 G, T_A = 25°C	–	1.5	–	V
		QVO_COARSE = 4, QVO_FINE = 0, Magnetic Input B = 0 G, T_A = 25°C	–	0.5	–	V
Quiescent Voltage Output Fine Range	$V_{OUT(Q)}$	QVO_COARSE = 0, Magnetic Input B = 0 G, T_A = 25°C	2	–	3	V
		QVO_COARSE = 1, Magnetic Input B = 0 G, T_A = 25°C	3	–	4	V
		QVO_COARSE = 2, Magnetic Input B = 0 G, T_A = 25°C	4	–	$V_{OUT(sat)H}$	V
		QVO_COARSE = 3, Magnetic Input B = 0 G, T_A = 25°C	1	–	2	V
		QVO_COARSE = 4, Magnetic Input B = 0 G, T_A = 25°C	$V_{OUT(sat)L}$	–	1	V
Quiescent Voltage Output Programming Bits	$BIT_{QVO\ COAR}$		–	3	–	bit
	$BIT_{QVO\ FINE}$		–	9	–	bit
Average Fine Quiescent Voltage Output Step Size [2][5][6]	$Step_{VOUT(Q)}$	T_A = 25°C	2.4	2.8	3	mV
Quiescent Voltage Output Programming Resolution [7]	$Err_{PG\ VOUT(Q)}$	T_A = 25°C	–	$Step_{VOUT(Q)}$ × 0.5	–	mV

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OPERATING CHARACTERISTICS (continued): Valid across full T_A range, C_{BYPASS} = 0.1 µF (internal), V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
SENSITIVITY PROGRAMMING						
Sensitivity Programming Bits	$BIT_{SENS\ COAR}$	Coarse (range selection)	–	2	–	bit
	$BIT_{SENS\ FINE}$	Fine (value selection)	–	9	–	bit
Typical Sensitivity for Coarse Adjustment	$Sens_{COARSE}$	SENS_COARSE = 0, SENS_FINE = 0, T_A = 25°C	–	1.67	–	mV/G
		SENS_COARSE = 1, SENS_FINE = 0, T_A = 25°C	–	3.35	–	mV/G
		SENS_COARSE = 2, SENS_FINE = 0, T_A = 25°C	–	6.34	–	mV/G
		SENS_COARSE = 3, SENS_FINE = 0, T_A = 25°C	–	12.12	–	mV/G
Sensitivity Fine Range	Sens	SENS_COARSE = 0, T_A = 25°C	1	–	1.94	mV/G
		SENS_COARSE = 1, T_A = 25°C	1.94	–	3.75	mV/G
		SENS_COARSE = 2, T_A = 25°C	3.75	–	7.28	mV/G
		SENS_COARSE = 3, T_A = 25°C	7.28	–	14.1	mV/G
Average Sensitivity Step Size [2][6][7]	$Step_{SENS}$	SENS_COARSE = 0, T_A = 25°C	3.6	4.5	5.7	µV/G
		SENS_COARSE = 1, T_A = 25°C	7.22	9.07	11.4	µV/G
		SENS_COARSE = 2, T_A = 25°C	13.7	17.2	21.6	µV/G
		SENS_COARSE = 3, T_A = 25°C	26.1	32.8	41.4	µV/G
Sensitivity Programming Resolution [7]	$Err_{PROG\ SENS}$	T_A = 25°C	–	±($Step_{SENS}$ × 0.5)	–	µV/G
POLARITY PROGRAMMING						
Directional Programming Bit [8]	BIT_{POL}		–	1	–	bit
ERROR COMPONENTS						
Linearity Sensitivity Error	Lin_{ERR}		–1	±0.5	1	%
Symmetry Sensitivity Error	Sym_{ERR}		–1	±0.5	1	%
Ratiometry Quiescent Voltage Output Error [9]	$Rat_{VOUT(Q)}$	Across supply voltage range (relative to V_{CC} = 5 V)	–0.5	±0.25	0.5	%
Ratiometry Sensitivity Error [9]	Rat_{SENS}	Across supply voltage range (relative to V_{CC} = 5 V)	–1	±0.5	1	%
Ratiometry Clamp Error [10]	$Rat_{VOUTCLP}$	T_A = 25°C, across supply voltage range (relative to V_{CC} = 5 V)	–0.5	±0.25	0.5	%

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OPERATING CHARACTERISTICS (continued): Valid across full T_A range, C_{BYPASS} = 0.1 µF (internal), V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ADDITIONAL CHARACTERISTICS						
Quiescent Voltage Output Drift Through Temperature Range [13]	$\Delta V_{OUT(Q)}$	SENS_COARSE = 0, 1, 2 or QVO_COARSE = 0, 1, 3	–20	–	+20	mV
		SENS_COARSE = 3 or QVO_COARSE = 2, 4	–30	–	+30	mV
Sensitivity Drift Error Through Temperature Range [14]	$\Delta Sens_{TC(ERR)}$	Programmed at T_A = 150°C	–2	–	2	%
Sensitivity Drift Error Due to Package Hysteresis	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling	–	±1.5	–	%
DIAGNOSTIC LEVELS						
Overvoltage Detection (Low)	$V_{CCOV(LOW)}$		7.6	8.2	8.6	V
Overvoltage Detection (High)	$V_{CCOV(HIGH)}$		8.6	9.2	9.6	V
Undervoltage Detection (Low)	$V_{CCUV(LOW)}$		3.7	3.9	4.1	V
Undervoltage Detection (High)	$V_{CCUV(HIGH)}$		3.9	4.1	4.3	V
Output Diagnostic Voltage	$V_{OUTDIAG}$		0.94 × V_{CC}	0.96 × V_{CC}	V_{CC}	V

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] See Characteristic Definitions.
[3] A 0.1 µF capacitor is located from VCC to GND and another from VOUT to GND within the package. Contact Allegro for manufacturer specifications.
[4] Value of characteristics before customer programming.
[5] Step size is larger than required, to account for manufacturing spread and temperature compensation. See Characteristic Definitions.
[6] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be twice the maximum specified value of $Step_{VOUT(Q)}$ or $Step_{SENS}$.
[7] Fine programming value accuracy. See Characteristic Definitions.
[8] Default polarity defined as increasing output voltage, V_{OUT}, in response to a positive (south polarity) field applied to the branded face of the device.
[9] Percent change from actual value at V_{CC} = 5 V, for a given temperature.
[10] Percent change from actual value at V_{CC} = 5 V, T_A = 25°C.
[11] Parameter not tested, maximum value determined from characterization only.
[12] For additional Pre-Programming Sensitivity Temperature Compensation values please contact Allegro MicroSystems.
[13] For combination of SENS_COARSE and QVO_COARSE, the wider specification applies.
[14] Sensitivity Drift is determined as deviation from the ideal Sensitivity at T_A. See Characteristic Definitions, Sensitivity Drift Through Temperature Range, for more information.

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CHARACTERISTIC DEFINITIONS

Power-On Time: When the supply is ramped to its operating voltage, the device requires a finite time to react to an input magnetic field. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within 90% of its final value in response to an applied magnetic field, as shown in Figure 1.

Delay to Clamp: A large magnetic input step may cause the clamp to overshoot its steady-state value. The Delay to Clamp, t_{CLP}, is defined as the time it takes for the output voltage to settle within 1% of its steady-state clamp voltage after initially passing through its steady-state voltage, as shown in Figure 2.

Propagation Delay: (t_{PD}) The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 3).

Response Time: ($t_{RESPONSE}$) The time interval between a) when the applied magnetic field reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied magnetic field (see Figure 4).

Quiescent Voltage Output: In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, equals a ratio of the supply voltage, V_{CC}, throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Quiescent Voltage Output Range: The Quiescent Voltage Output, $V_{OUT(Q)}$, can be programmed around 2.5 V within the Quiescent Voltage Output Range limits, $V_{OUT(Q)}$(min) and $V_{OUT(Q)}$(max). The available programming range falls within the distribution of the initial $V_{OUT(Q)}$ and the Max Code $V_{OUT(Q)}$, as shown in Figure 5.

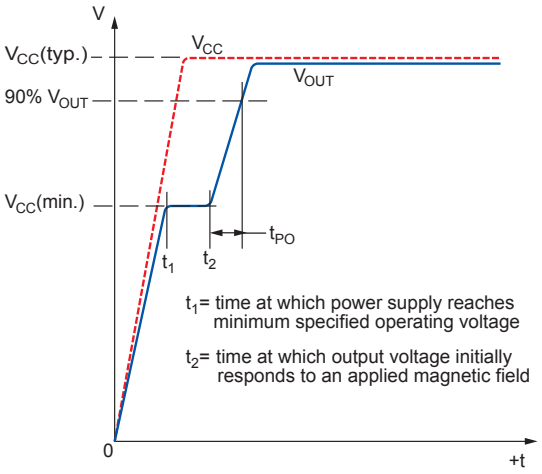

Figure 1: Power-On Time definition

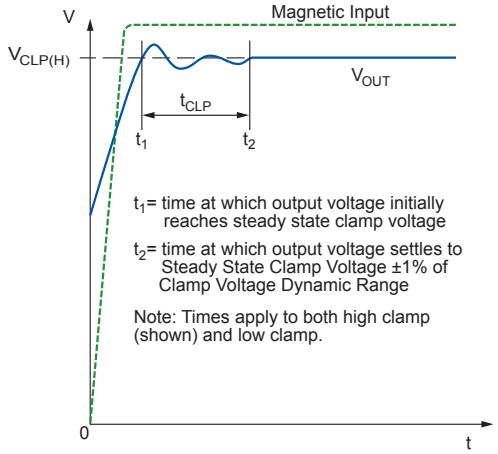

Figure 2: Delay to Clamp Definition

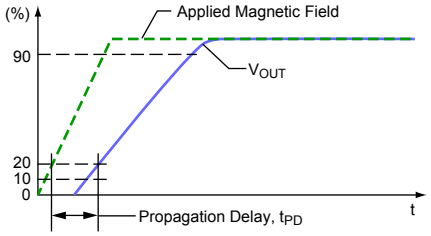

Figure 3: Propagation Delay Definition

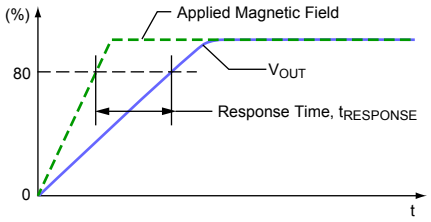

Figure 4: Response Time Definition

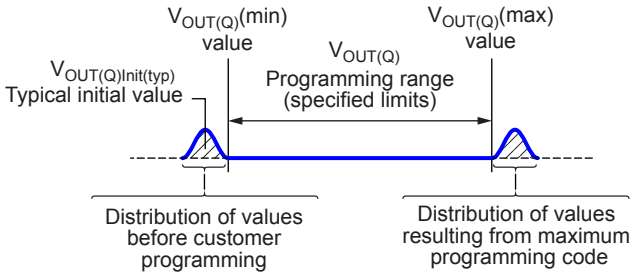

Figure 5: Quiescent Voltage Output Range Definition

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Average Quiescent Voltage Output Step Size: The average quiescent voltage output step size for a single device is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)max} - V_{OUT(Q)min}}{n} \quad , \qquad (1)$$

where *n* is the recommended available programming range, in LSBs. For purposes of specification, *n* is defined as 447.

Quiescent Voltage Output Programming Resolution: The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$0.5 \times Step_{VOUT(Q)}(typ) \qquad (2)$$

Quiescent Voltage Output Drift Through Temperature Range: Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output, $V_{OUT(Q)}$, may drift from its nominal value through the operating ambient temperature range, T_A. The Quiescent Voltage Output Drift Through Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)T_A} - V_{OUT(Q)25°C} \qquad (3)$$

Sensitivity: The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, defined as:

$$Sens = \frac{\Delta V_{OUT}}{\Delta B} \quad , \qquad (4)$$

where ΔB is the change in applied magnetic field corresponding to ΔV_{OUT}.

Sensitivity Range: The magnetic sensitivity can be programmed around its initial value within the sensitivity range limits, Sens(min) and Sens(max). Refer to the Quiescent Voltage Output Range section for a conceptual explanation.

Average Sensitivity Step Size: Refer to the Average Quiescent Voltage Output Programming Step Size section for a conceptual explanation.

Sensitivity Programming Resolution: Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient: Device sensitivity changes as temperature changes, with respect to its sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is factory-programmed, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{SENS} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\ (\%)\right)\left(\frac{1}{T2–T1}\right) \qquad (5)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The ideal value of Sens through the full ambient temperature range, $Sens_{IDEAL(T_A)}$, is defined as:

$$Sens_{IDEAL(T_A)} = Sens_{T1} \times [100\ (\%) + TC_{SENS}\ (T_A - T1)] \quad . \qquad (6)$$

Sensitivity Temperature Coefficient Range: The magnetic sensitivity temperature coefficient can be programmed within its limits of TC_{Sens}(max) and TC_{Sens}(min). Refer to the Quiescent Voltage Output Range section for a conceptual explanation.

Average Sensitivity Temperature Coefficient Step Size: Refer to the Average Quiescent Voltage Output Step Size section for a conceptual explanation.

Sensitivity Temperature Coefficient Programming Resolution: Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Drift Through Temperature Range: The Sensitivity drift is factory-trimmed to best approximate an ideal linear function. The ideal Sensitivity drift function is specified by the characteristic Pre-Programming Sensitivity Temperature Compensation, and is typically selected to compensate for losses common with certain magnet materials. For example, the temperature compensation, $TC3_{SENS}$, is commonly used in systems when paired with a SmCo type rare-earth magnet. Non-ideal errors cause the Sensitivity drift to deviate from its ideal value across

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the operating ambient temperature range, T_A. Figure 6 shows the Sensitivity drift for compensation settings $TC1_{SENS}$ and $TC3_{SENS}$. The gray area represents the minimum and maximum Senstivity Drift Error, $\Delta Sens_{TC(ERR)}$.

For purposes of specification, the Sensitivity Drift Through Temperature Range, ΔSensTC, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{IDEAL(TA)}}{Sens_{IDEAL(TA)}} \times 100\ (\%) \quad . \quad (7)$$

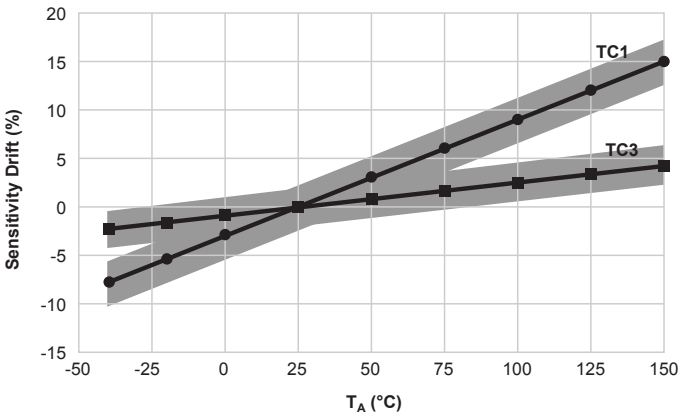

Figure 6: Sensitivity Drift Through Temperature Range (ΔSensTC)

Sensitivity Drift Due to Package Hysteresis: Package stress and relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling. This change in sensitivity follows a hysteresis curve, shown in Figure 7. For purposes of specification, the Sensitivity Drift Due to Package Hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\ (\%) \quad , \quad (8)$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 150°C, down to –40°C and back up to 25°C.

Linearity Sensitivity Error: The A1377 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

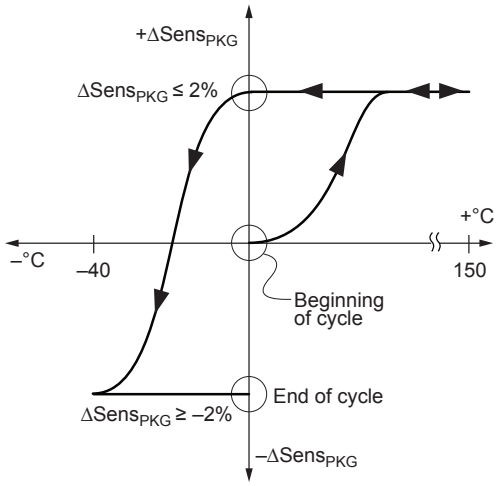

Figure 7: Package Hysteresis Sensitivity Drift During Temperature Cycling

Linearity Error: is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\ (\%) \quad ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\ (\%) \quad , \quad (9)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \quad (10)$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = 2 × |BPOS1| and |BNEG2| = 2 × |BNEG1|.

Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \quad (11)$$

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The output voltage clamps, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, limit the operating magnetic range of the applied field in which the device provides a linear output. The maximum positive and negative applied magnetic fields in the operating range can be calculated:

$$|B_{MAXPOS}| = \frac{V_{CLP(HIGH)} - V_{OUT(Q)}}{Sens},$$

$$|B_{MAXNEG}| = \frac{V_{OUT(Q)} - V_{CLP(LOW)}}{Sens}, \quad (12)$$

Although the application of very large magnetic fields does not damage these devices, such fields will affect the clamps by forcing the output into a nonlinear region (Figure 8).

Symmetry Sensitivity Error: The magnetic sensitivity of an A1377 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100 \ (\%), \quad (13)$$

where $Sens_{Bx}$ is as defined in equation 10, and BPOS and BNEG are positive and negative magnetic fields such that |BPOS| = |BNEG|.

Ratiometry Error: The A1377 device features ratiometric output. This means that the Quiescent Voltage Output, $V_{OUT(Q)}$, magnetic sensitivity, Sens, and clamp voltages, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, are proportional to the supply voltage. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$\%Rat_{ERRVOUT(Q)}(V_{CC}) = \left(\frac{V_{OUT(Q)}(V_{CC})}{V_{CC}} - \frac{V_{OUT(Q)}(5\ V)}{5\ V}\right) \times 100 \quad (14)$$

where $V_{OUT(Q)}(V_{CC})$ is the quiescent output voltage at the supply voltage = V_{CC}, and $V_{OUT(Q)}(5\ V)$ is the quiescent output voltage at the supply voltage = 5 V.

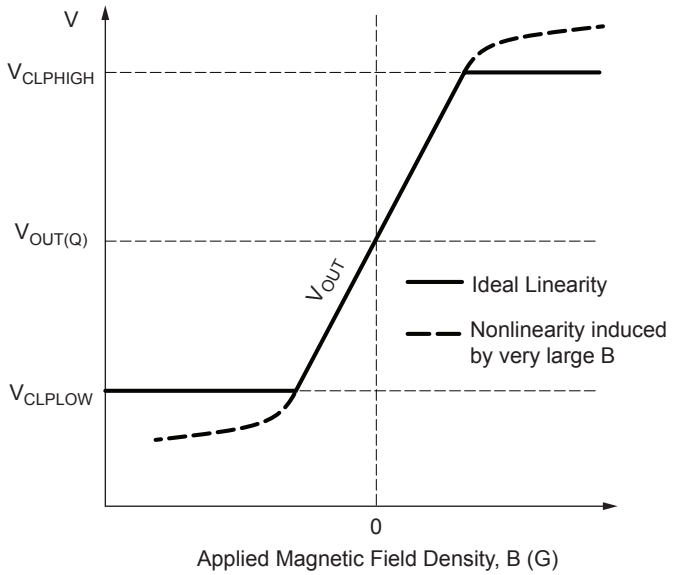

Figure 8: Ideal Linear Clamping Behavior and Nonlinearity Forced by Large Applied Magnetic Field

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given Supply Voltage, V_{CC}, is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)}/Sens_{(5\ V)}}{V_{CC}/5\ V}\right) \times 100\ (\%) \quad (15)$$

The ratiometric error in the clamp voltages, $Rat_{VOUTCLP}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$\%Rat_{ERRVOUTCLP(Q)}(V_{CC}) = \left(\frac{V_{CLP}(V_{CC})}{V_{CC}} - \frac{V_{CLP}(5\ V)}{5\ V}\right) \times 100 \quad (16)$$

where $V_{CLP}(V_{CC})$ is the output at the clamp voltage when the supply voltage = V_{CC}, and $V_{CLP}(5\ V)$ is the output at the clamp voltage the supply voltage = 5 V. The clamp voltage is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

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FUNCTIONAL DESCRIPTION

Diagnostic Conditions

Application circuits to implement A1377 diagnostic outputs are shown in Figure 9. The interpretation of diagnostic outputs is provided in Table 1.

Undervoltage Detection

The A1377 contains circuitry to detect a condition in which the supply voltage drops below the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{CCUV(HIGH)} - V_{CCUV(LOW)}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} drops below $V_{CCUV(LOW)}$, V_{OUT} is pulled up to V_{DIAG}. When V_{CC} returns above $V_{CCUV(HIGH)}$, V_{OUT} returns to its normal operating state after a delay of approximately Power-On Time, t_{PO}.

Overvoltage Detection

The A1377 contains circuitry to detect a condition in which the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{CCOV(HIGH)} - V_{CCOV(LOW)}$.

As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} rises above $V_{CCOV(HIGH)}$, V_{OUT} is pulled up to $V_{OUTDIAG}$. When V_{CC} returns below $V_{CCOV(LOW)}$, V_{OUT} returns to its normal operating state. The delay is approximately the same as t_e, described in the Programming Guidelines section.

Broken Ground Detection

The A1377 contains circuitry to detect a condition in which the ground connection is disconnected. It forces the output to a known diagnostic state: when a broken ground is detected, V_{OUT} rises to $V_{OUTDIAG}$.

EEPROM Diagnostics

The A1377 contains EEPROM with error checking and correction, ECC. The ECC corrects for a single-bit EEPROM error without affecting device performance. The ECC also detects a dual-bit EEPROM error and triggers an internal fault signal that disables the output to a high-impedance state. If a single- or dual-bit EEPROM error occurs, a diagnostic flag is set in a register.

EEPROM Margin Checking

The A1377 contains a test mode, called EEPROM Margining, to check the logic levels of the EEPROM bits. EEPROM margining is accessible with customer EEPROM access. EEPROM margining is selectable to check all logic 1 bits, logic 0 bits, or both. To run EEPROM Margining—checking both logic 1 and logic 0 bits for the entire EEPROM—write MARGIN_START in address TEST_C, 0x10, to logic 1. The results of the test are reported back in EEPROM registers MRGNF_C, 0x11, and ECCF_C, 0x12. For more EEPROM Margining information and options, refer to the table Memory Address Map.

Note: A fail of EEPROM Margining does not force the output to a diagnostic state.

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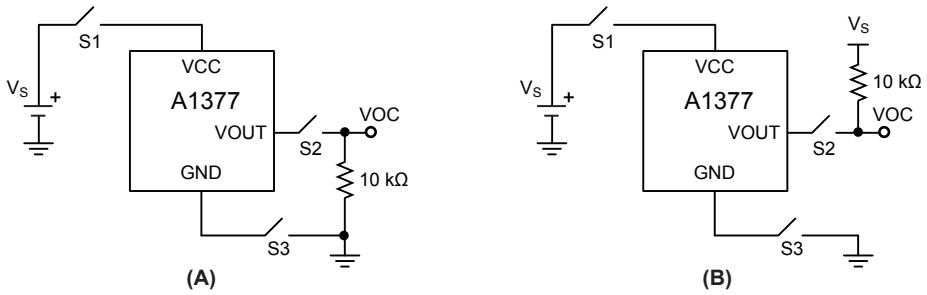

Figure 9: Diagnostic Application Circuits: (A) Pull-Down, (B) Pull-Up

Table 1: Diagnostic Detection Conditions Truth Table

Description	Circuit	S1	S2	S3	VOUT	VOC
Broken VCC	A	Open	Closed	Closed	High Impedance	GND
	B					V_{CC}
Broken VOUT	A	Closed	Open	Closed	Low Impedance	GND
	B					V_{CC}
Broken Ground	A	Closed	Closed	Open	Low Impedance	$V_{OUTDIAG}$
	B					
EEPROM Fault (2-bit error detection)	A	Closed	Closed	Closed	High Impedance	GND
	B					V_{CC}
Overvoltage Condition	A	Closed	Closed	Closed	Low Impedance	$V_{OUTDIAG}$
	B					
Undervoltage Condition	A	Closed	Closed	Closed	Low Impedance	$V_{OUTDIAG}$
	B					

Note: For proper diagnostic detection, the device output clamps should be programmed to appropriate levels. Typical levels are 0.5 V for clamp low and 4.5 V for clamp high.

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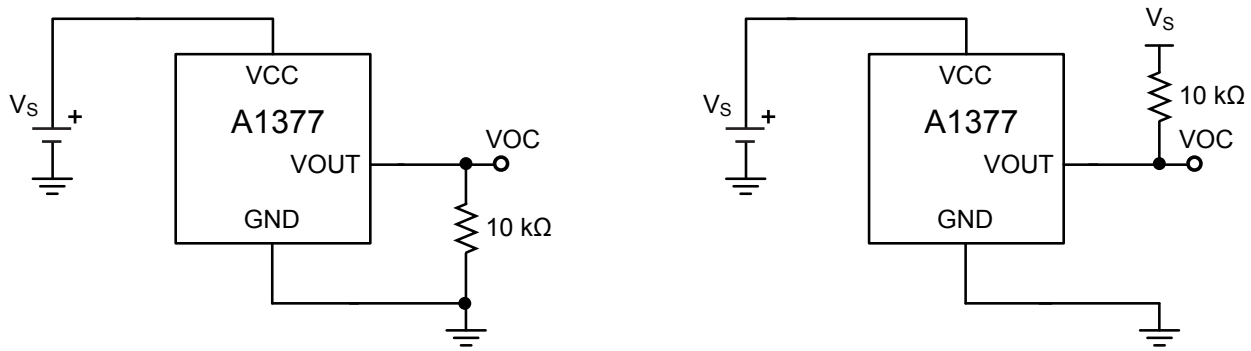
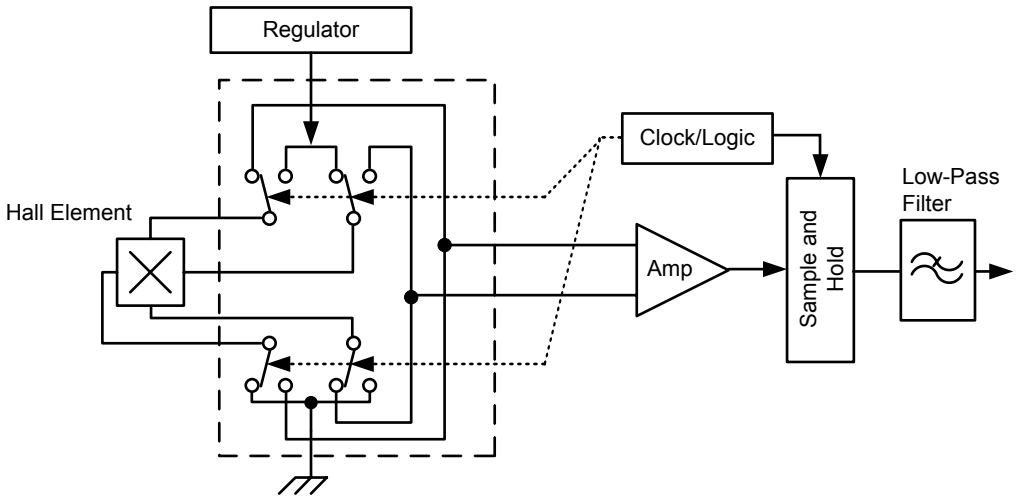
APPLICATION INFORMATION



Typical Application Circuits

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output across the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a high-frequency clock, f_C. For demodulation process, a sample-and-hold technique is used, where the sampling is performed at twice the chopper frequency ($f_C \times 2$). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

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PROGRAMMING GUIDELINES

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the A1377 using a point-to-point command/acknowledge protocol. The A1377 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the A1377. If the command is a read, the A1377 responds by transmitting the requested data.

Serial interface timing parameters can be found in the Programming Levels table, below. Note that the external controller must avoid sending a Command frame that overlaps a Read Acknowledge frame.

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the A1377: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the A1377 in response to a Read command.

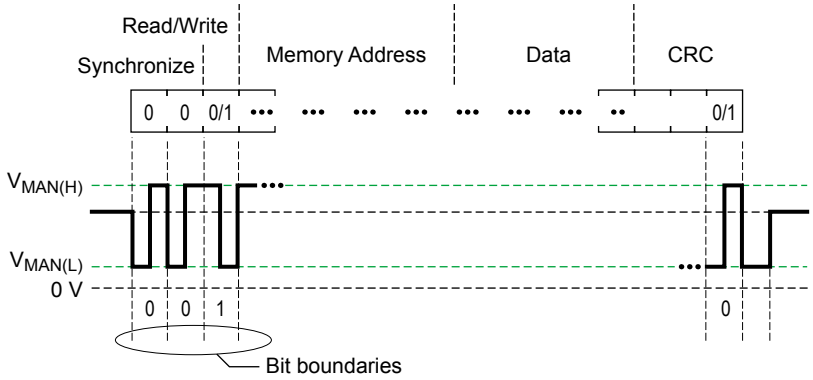

Figure 10: General Format for Serial Interface Commands

Programming Parameters, C_{LX} = 0

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Program Enable Voltage (High)	V_{prgH}	Program enable signal high level on VCC	8	–	8.5	V
Program Enable Voltage (Low)	V_{prgL}	Program enable signal low level on VCC	4.5	–	6	V
Output Enable Delay	t_e	External capacitance (C_{LX}) on VOUT may increase the Output Enable Delay	–	125	–	µs
Program Time Delay	t_d		–	–	500	µs
Program Write Delay	t_w		–	20	–	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT	4.0	–	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT	0	–	1	V
Bit Rate		Communication rate	250	–	2000	bit/s

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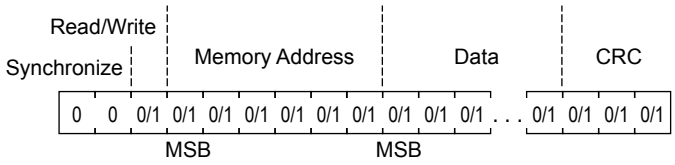
The A1377 device uses a three-wire programming interface, where VCC is used to control the program enable signal, data is transmitted on VOUT, and all signals are referenced to GND. This three-wire interface makes it possible to communicate with multiple devices with shared VCC and GND lines.

The four transactions (Write Access, Write to EEPROM, Write to Volatile Memory, and Read) are show in the figures on the following pages. To initialize any communication, VCC should be increased to a level above V_{prgH}(min) without exceeding V_{prgH}(max). At this time, VOUT is disabled and acts as an input.

After program enable is asserted, the external controller must drive the output low in a time less than t_d. This prevents the device interpreting any false transients on VOUT as data pulses. After the command is completed, V_{CC} is reduced below V_{prgL}, back to normal operating level. Also, the output is enabled and responds to magnetic input.

When performing a Write to EEPROM transaction, the A1377 requires a delay of t_w to store the data into the EEPROM. The device will respond with a high-to-low transition on VOUT to indicate the Write to EEPROM sequence is complete.

When sending multiple command frames, it is necessary to toggle the program enable signal on VCC. After the first command frame is completed, and V_{CC} remains at V_{prgH}, the device will ignore any subsequent pulses on the output. When the program enable signal is brought below $V_{prgL(max)}$, the output will respond to the magnetic input. To send the next command, the program enable signal is increased to V_{prgH}.



Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
30	Data	0/1	24 data bits and 6 ECC bits. For a read command frame the data consists of 30 bits: [29:26] Don't Care, [25:24] ECC Pass/Fail, and [23:0] Data. Where bit 0 is the LSB. For a write command frame the data consists of 30 bits: [29:24] Don't Care and [23:0] Data. Where bit 0 is the LSB.
3	CRC	0/1	Bits to check the validity of frame.

Figure 11: Command Frame General Format

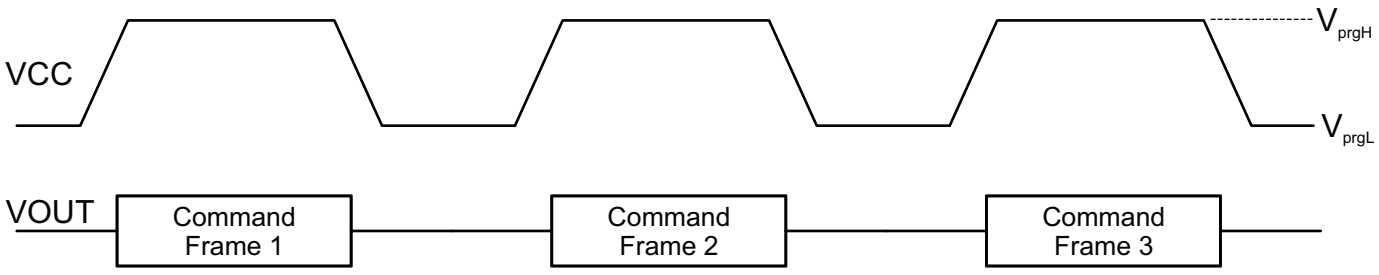


Figure 12: Format for Sending Multiple Transactions

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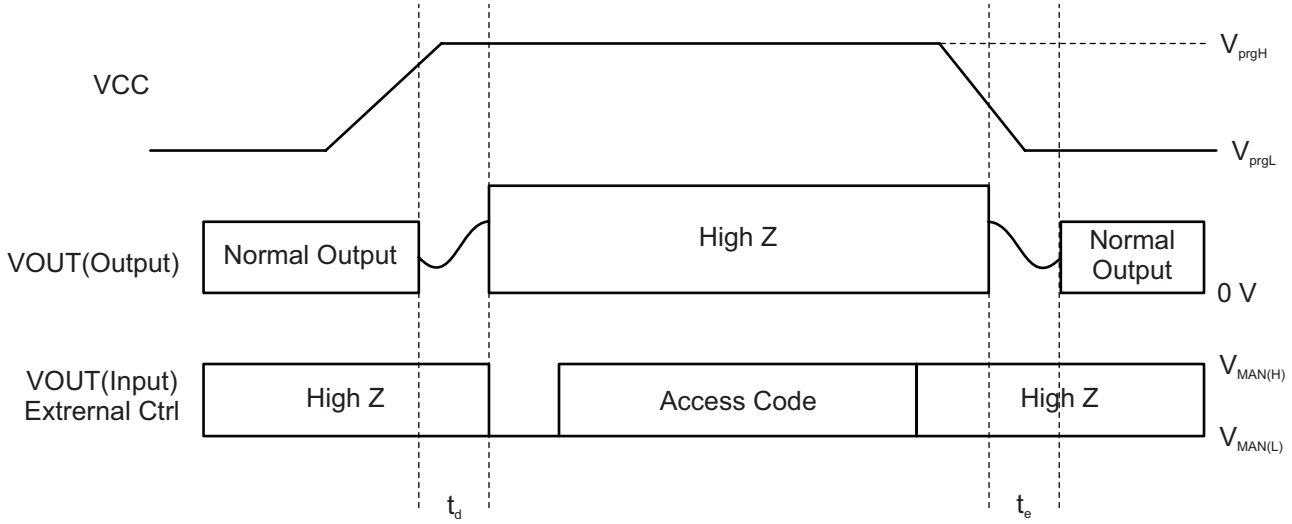

Figure 13: Write Access Code

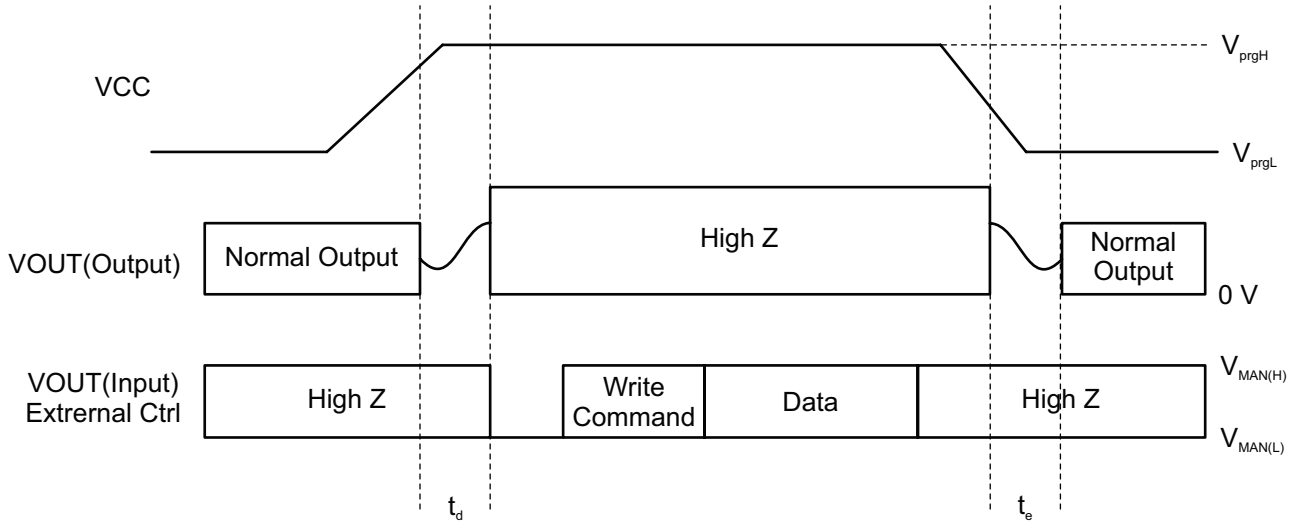

Figure 14: Write to Volatile Memory

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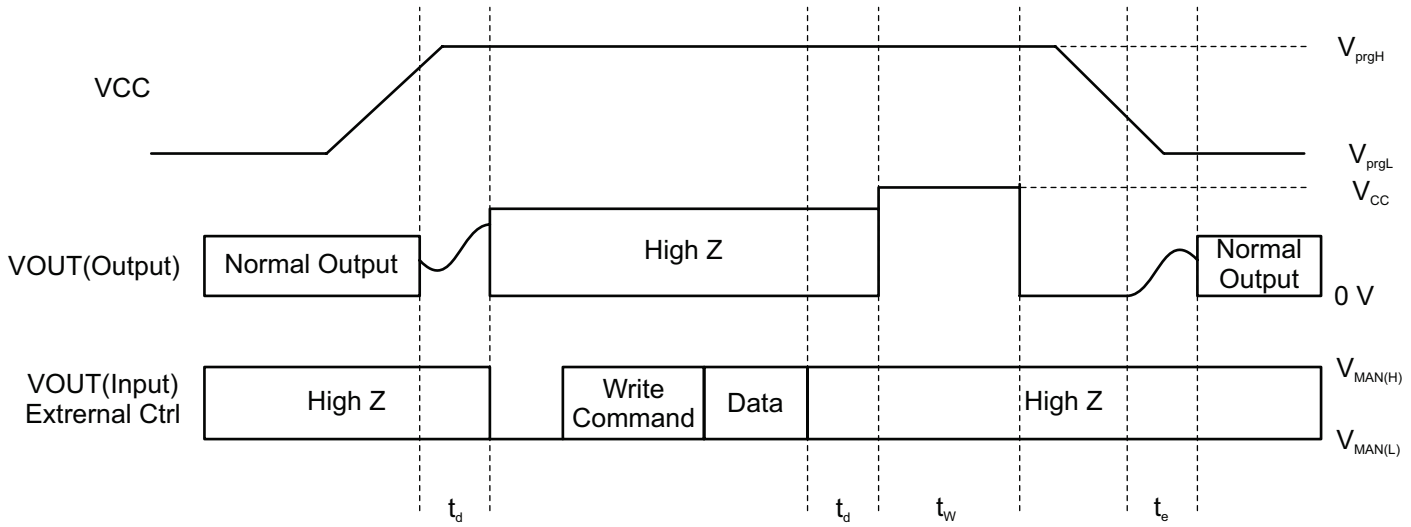

Figure 15: Write to Non-Volatile Memory (EEPROM)

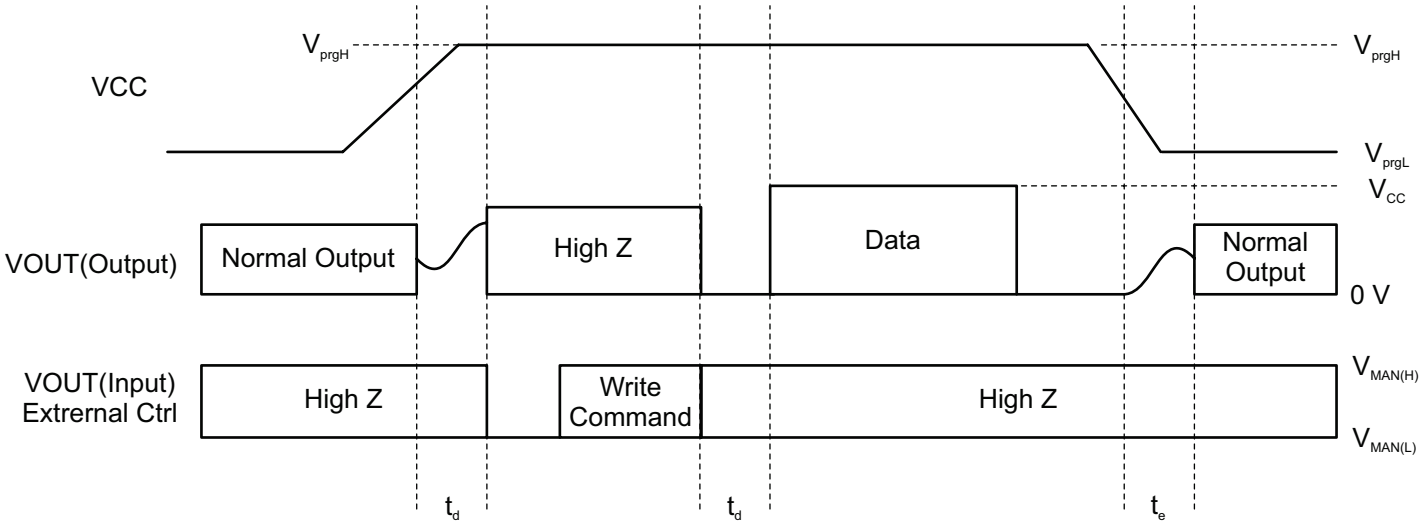

Figure 16: Read

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Table 2: Memory Address Map

Type	ADDR	Register Name	Parameter Name	Description	R/W	Bits	Location
EEPROM Customer Read Only	0x00	WLOT_F	FACTORY_LOT	Factory Lot	RW[1]	16	15:0
			FACTORY_WAFER	Factory Wafer	RW[1]	6	21:16
			Unused	Factory Use Only	RW[1]	2	23:22
	0x01	ID_F	X_DIE_LOC	8 bits X die location	RW[1]	8	7:0
			Y_DIE_LOC	8 bits Y die location	RW[1]	8	15:8
			PTEST	Bits reserved for additional factory tracking	RW[1]	8	23:16
EEPROM Customer	0x02	ID_C	CUST_ID		RW	24	23:0
	0x03	SENS_C	SENS_FINE	Sensitivity, fine adjustment	RW	9	8:0
			SENS_COARSE	Sensitivity, coarse adjustment	RW	2	10:9
			POL	Reverses Sensitivity polarity	RW	1	11
			RESERVED	Reserved	RW	9	20:12
			RESERVED	Reserved	RW	2	22:21
			RESERVED	Reserved	RW	1	23
	0x04	QVO_C	QVO_FINE	Quiescent Output Voltage (QVO), fine adjustment	RW	9	8:0
			QVO_COARSE	Course QVO adjustment	RW	3	11:9
			RESERVED	Reserved	RW	9	20:12
			RESERVED	Reserved	RW	3	23:21
	0x05	CLAMP_C	CLAMP_LOW	Lower Output Clamp	RW	9	8:0
			Unused		RW	3	11:9
			CLAMP_HIGH	Upper Output Clamp	RW	9	20:12
			Unused		RW	3	23:21
	0x06	COMCFG_C	DEV_LOCK	Bit to set the EELOCK	RW	1	0
			Unused		RW	10	10:1
			Unused		RW	12	23:11
EEPROM Factory	0x07		Factory Only		R	24	23:0
	0x08		Factory Only		R	24	23:0
	0x09		Factory Only		R	24	23:0
	0x0A		Factory Only		R	24	23:0
	0x0B		Factory Only		R	24	23:0
	0xC		Factory Only		R	24	23:0
	0xD		Factory Only		R	24	23:0
	0xE		Factory Only		R	24	23:0
	0xF		Factory Only		R	24	23:0

Continued on the next page…

[1] Customer Access restricted to read only.

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Table 2: Memory Address Map (continued)

Type	ADDR	Register Name	Parameter Name	Description	R/W	Bits	Location
StaticCustomer	0x10	TEST_C	SHAWDOW_EN	Enables register shadowing for direct writes to shadowed (volatile) EEPROM registers	RW	1	0
			DISANALOG_OUT	Turns off the analog output for serial communications	RW	1	1
			CUSTOMER_ ACCESS	Indicates customer write access enabled	R	1	2
			Unused		R	1	3
			MARGIN_START	Write to 1 to start margin testing. If EE_LOOP is low, this bit will self clear when address 0xB is reached. If EE_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.	RW	1	4
			NO_MARGIN_MAX	0: Max reference voltage will be used during margin testing 1: Max voltage reference will be skiped during margin testing	RW	1	5
			NO_MARGIN_MIN	0: Min reference voltage will be used during margin testing 1: Min voltage reference will be skiped during margin testing	RW	1	6
			Unused		RW	1	7
			EE_STR_ADDR	If USE_TST_ADDR is set, then margining will start at this address. If magining fails, this will contain the failing address.	RW	4	11:8
			USE_STR_ADDR	0: No effect 1: Uses EE_TST_ADDR as the start address for margining. If EE_LOOP is set, this bit is ignored and the starting address is always 0x0	RW	1	12
			EE_LOOP	0: Test completes at address 0xB or fail 1: Test loops until MARGIN_START is written low or fail	RW	1	13
			Unused		R	10	23:14
	0x11	MRGNF_C	EE_TST_DATA	If margining fails, this is the failed data read from EEPROM.	R	24	23:0
	0x12	ECCF_C	EE_TST_ECC	If margining fails, this is the failed ECC read from EEPROM.	R	6	5:0
			Unused		R	2	7:6
			EE_TST_ADDR	If margining fails, this is the failed address from EEPROM.	R	4	11:8
			MARGIN_STATUS	00_2: Reset condition (no result from margin testing) 01_2: Pass, no failure detected during margin testing 10_2: Fail, failure detected during margin testing 11_2: Running, margin test is still running	R	2	13:12
			MIN_MAX_FAIL	If margining fails, this bit indicates if the min or max reference failed. 0: Min margining failed. 1: Max margining failed.	R	1	14
			Unused		R	14	23:15

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PROGRAMMABLE PARAMETER REFERENCE

Table 3: CLAMP_HIGH: Address 0x05 bits 20:12

Function	Sets level for upper output clamp
Syntax	Quantity of bits: 9
Related Commands	CLAMP_LOW
Values	0x0: Default, Output is at $V_{CLP(HIGH)}$(max) 0x1FF: Upper clamp is below $V_{CLP(HIGH)}$(min)
Options	
Examples	

Table 4: CLAMP_LOW: Address 0x05 bits 8:0

Function	Sets level for lower output clamp
Syntax	Quantity of bits: 9
Related Commands	CLAMP_HIGH
Values	0x0: Default, Output is at $V_{CLP(LOW)}$(min) 0x1FF: Lower clamp is above $V_{CLP(LOW)}$(max)
Options	
Examples	

Table 5: CUST_ID: Address 0x02 bits 23:0

Function	Bits available for custom ID programming
Syntax	Quantity of bits: 24
Related Commands	
Values	
Options	
Examples	Values are customer defined and do not effect device operation

Table 6: DEV_LOCK: Address 0x06 bit 0

Function	Bit to disable serial communication. When set, read and write access is disabled.
Syntax	Quantity of bits: 1
Related Commands	
Values	0x0: Default, Serial communication enabled 0x1: Serial communication disabled
Options	
Examples	When set the Program Enable threshold is ignored and the device output remains ratiometric until V_{CC} exceeds $V_{CCOV(HIGH)}$. This should only be applied after programming is complete and verified.

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Table 7: POL: Address 0x03 bit 11

Function	Bit to set the Sensitivity polarity
Syntax	Quantity of bits: 1
Related Commands	SENS_FINE, SENS_COARSE
Values	0x0: Default, Positive 0x1: Negative
Options	
Examples	See Characteristic Definitions, Sensitivity

Table 8: QVO_COARSE: Address 0x04 bits 11:9

Function	Coarse QVO adjustment
Syntax	Quantity of bits: 3
Related Commands	QVO_FINE
Values	0x0: Default, $V_{OUT(Q)}$ adjustable range defined by QVO_COARSE = 0 0x1: $V_{OUT(Q)}$ adjustable range defined by QVO_COARSE = 1 0x2: $V_{OUT(Q)}$ adjustable range defined by QVO_COARSE = 2 0x3: $V_{OUT(Q)}$ adjustable range defined by QVO_COARSE = 3 0x4: $V_{OUT(Q)}$ adjustable range defined by QVO_COARSE = 4 0x5: Not used 0x6: Not used 0x7: Not used
Options	
Examples	See Operating Characteristics

Table 9: QVO_FINE: Address 0x04 bits 8:0

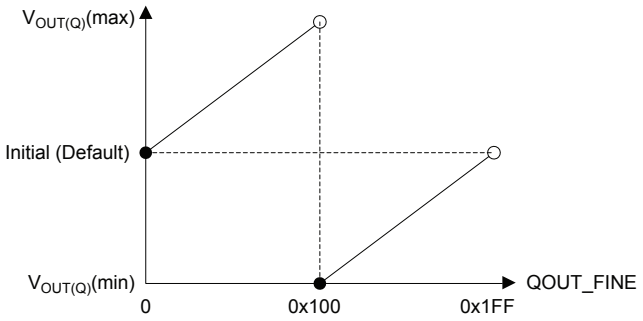
Function	Fine QVO adjustment
Syntax	Quantity of bits: 9 Signed
Related Commands	QVO_COARSE
Values	
Options	
Examples	Fine adjustment of $V_{OUT(Q)}$, range defined by QVO_COARSE; see Operating Characteristics

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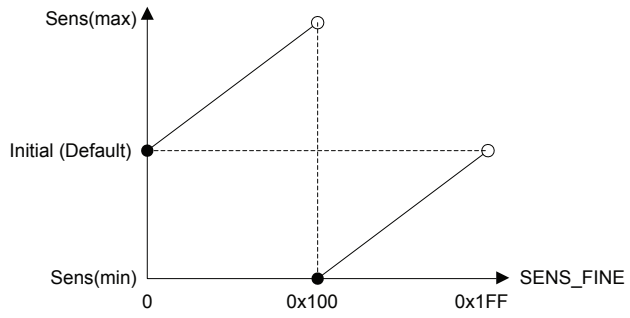
Table 10: SENS_COARSE: Address 0x03 bits 10:9

Function	Coarse Sensitivity adjustment
Syntax	Quantity of bits: 2
Related Commands	SENS_FINE, POL
Values	0x0: Default, Sens adjustable range defined by SENS_COARSE = 0 0x1: Sens adjustable range defined by SENS_COARSE = 1 0x2: Sens adjustable range defined by SENS_COARSE = 2 0x3: Sens adjustable range defined by SENS_COARSE = 3
Options	
Examples	See Operating Characteristics

Table 11: SENS_FINE: Address 0x03 bits 8:0

Function	Fine Sensitivity adjustment
Syntax	Quantity of bits: 9 Signed
Related Commands	SENS_COARSE, POL
Values	
Options	
Examples	Fine adjustment of Sens, range defined by SENS_COARSE; see Operating Characteristics

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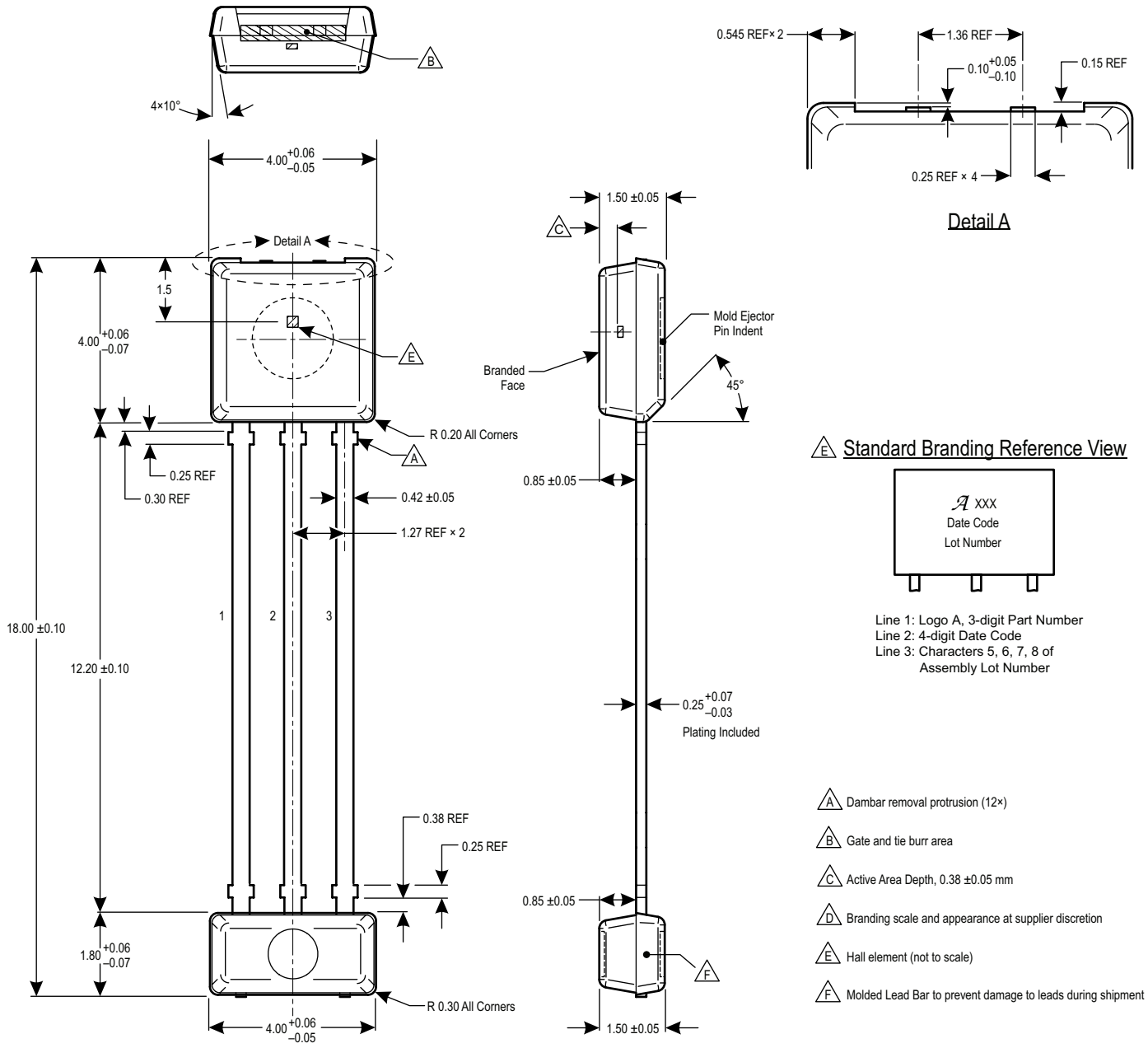
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000409, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Package UC, 3-Pin SIP

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Revision History

Revision	Date	Description
–	April 21, 2016	Initial release
1	May 10, 2016	Corrected Features and Benefits; Added test condition to t_{pd} and $t_{RESPONSE}$; Updated Quiescent Voltage Output Drift Through Temperature Range test condition and footnote; Added EEPROM Margining under Functional Description; Corrected Figure 6
2	February 22, 2019	Minor editorial updates
3	July 8, 2022	Updated package drawing (page 24) and minor editorial updates

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